Title: SUBSTRATE FOR A LIQUID CRYSTAL DEVICE, METHOD OF MANUFACTURING A SUBSTRATE FOR A LIQUID CRYSTAL DEVICE, A LIQUID CRYSTAL DEVICE, A METHOD OF MANUFACTURING A LIQUID CRYSTAL DEVICE, AND AN ELECTRONIC APPARATUS
Inventor: TADASHI TSUYUKI, ET AL.
Atty. Ref. No.: 9319S-000308

Fig. 1

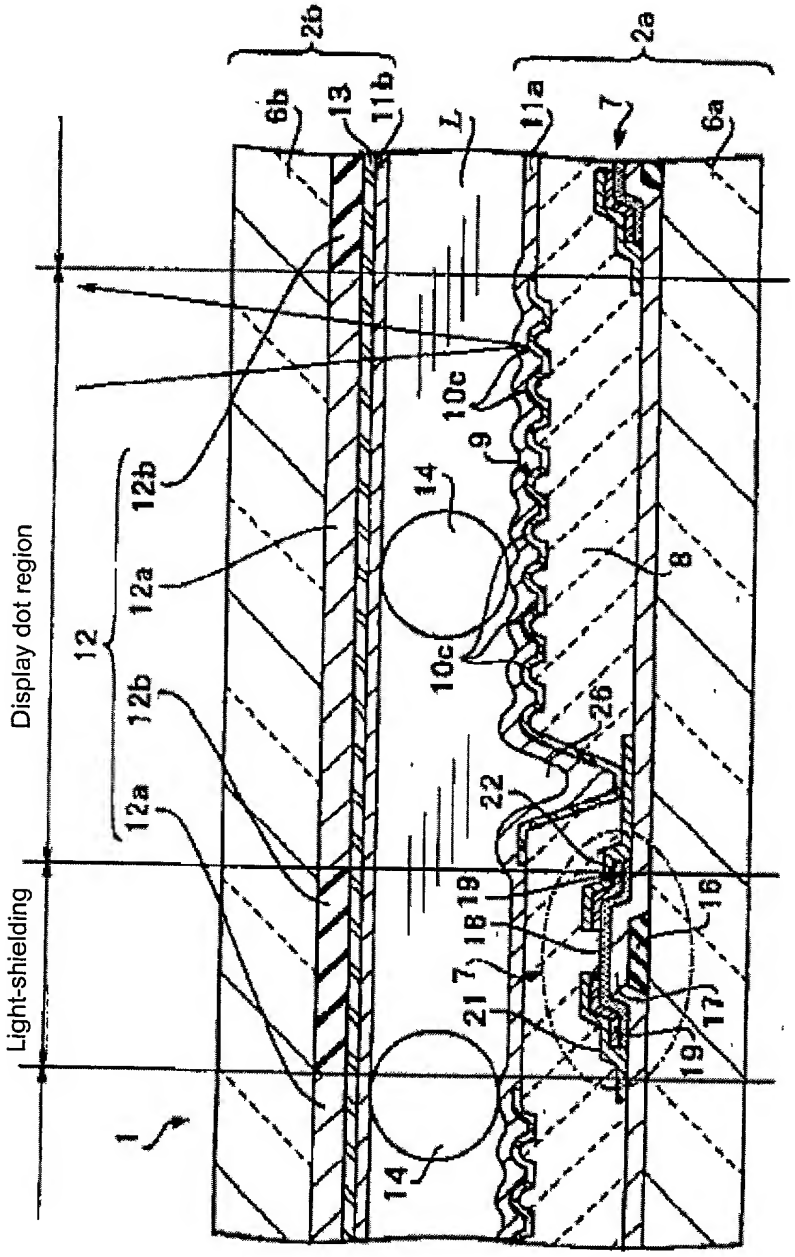


Fig.2

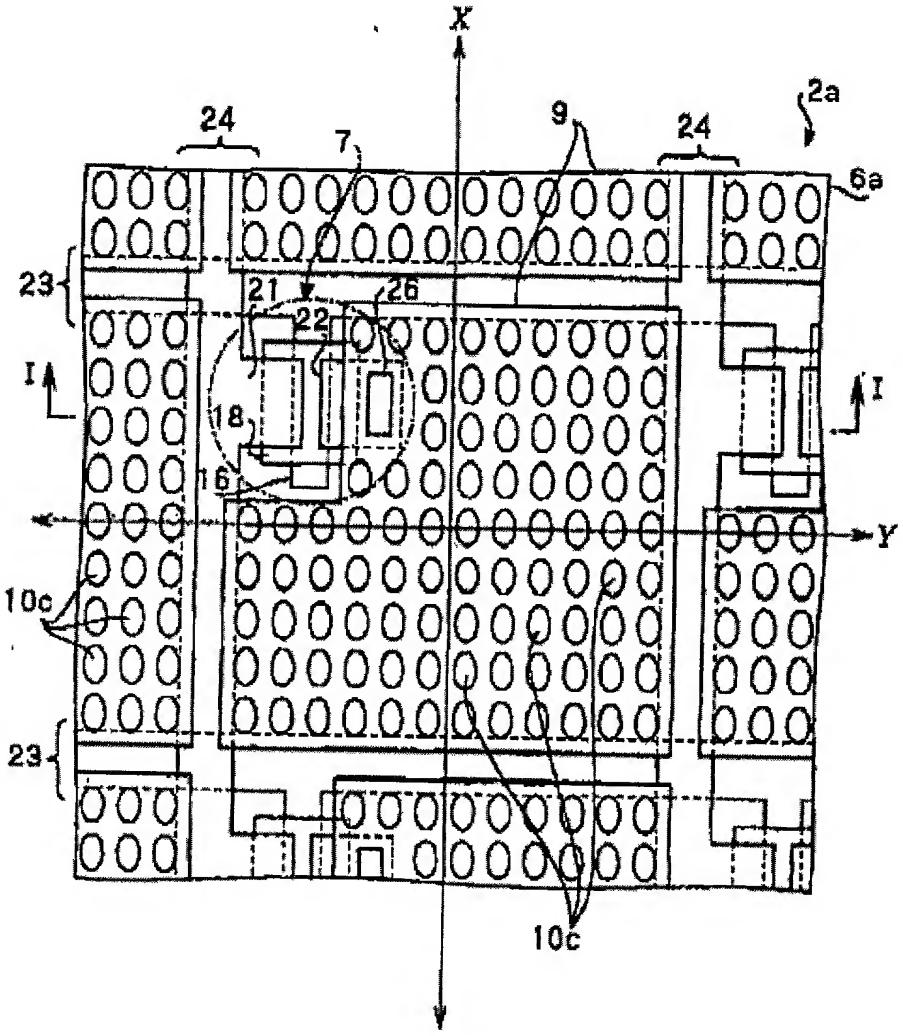


Fig. 3

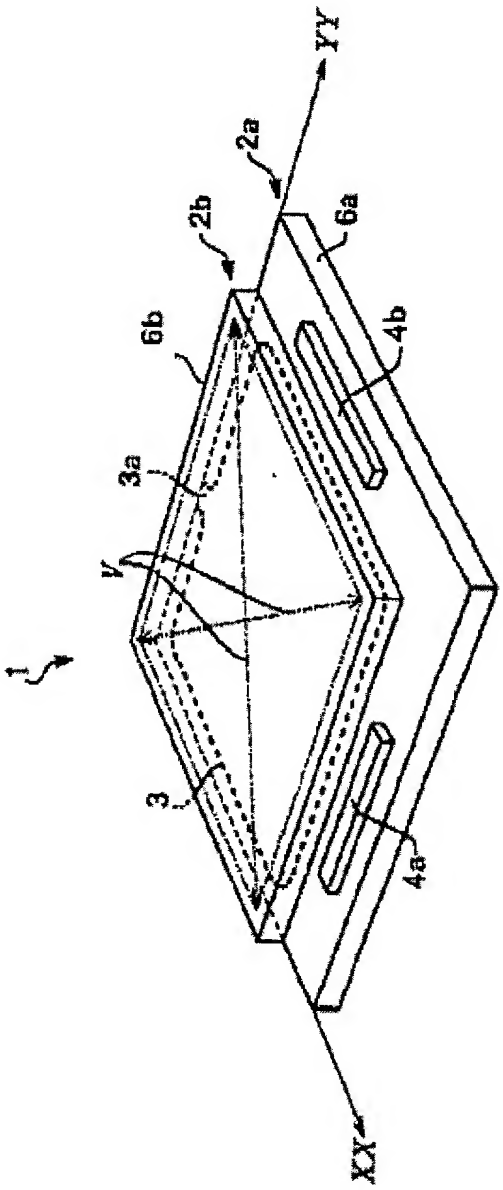


Fig. 4

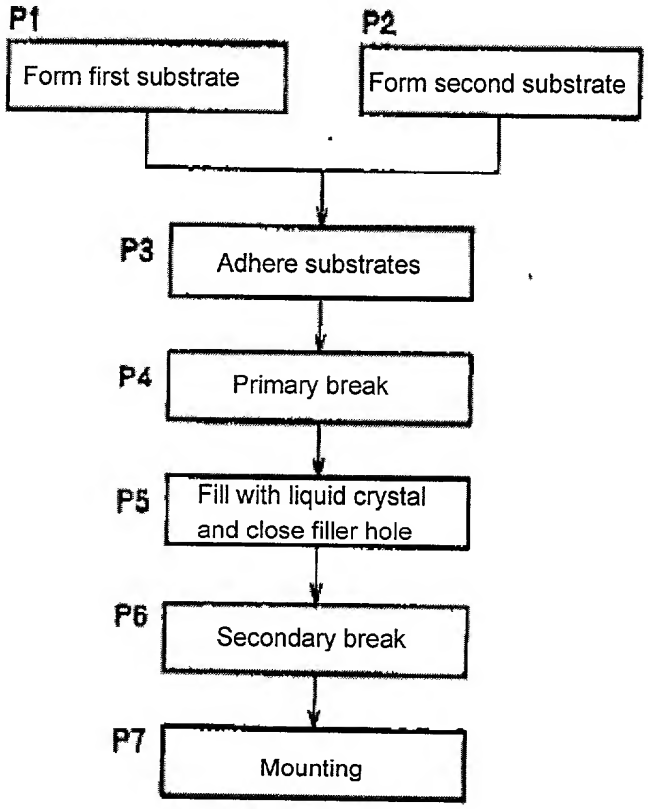

P1
Form first substrate
P2
Form second substrate
P3
Adhere substrates
P4
Primary break
P5
Fill with liquid crystal and close filler hole
P6
Secondary break
P7
Mounting

Fig. 5

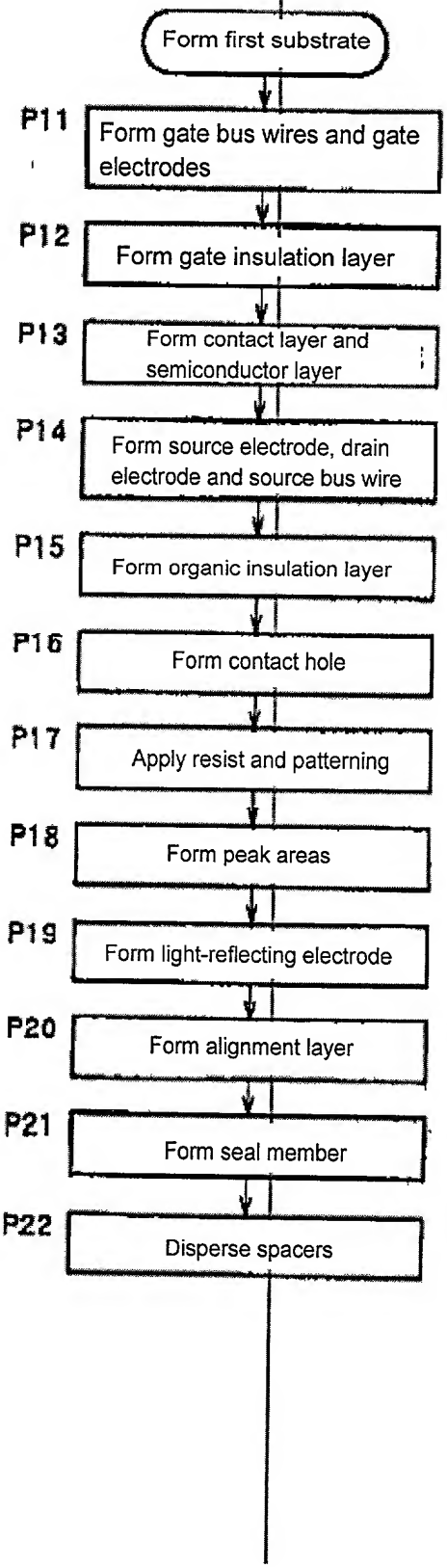

Form first substrate
P11
Form gate bus wires and gate electrodes
P12
Form gate insulation layer
P13
Form contact layer and semiconductor layer
P14
Form source electrode, drain electrode and source bus wire
P15
Form organic insulation layer
P16
Form contact hole
P17
Apply resist and patterning
P18
Form peak areas
P19
Form light-reflecting electrode
P20
Form alignment layer
P21
Form seal member
P22
Disperse spacers

Fig. 6

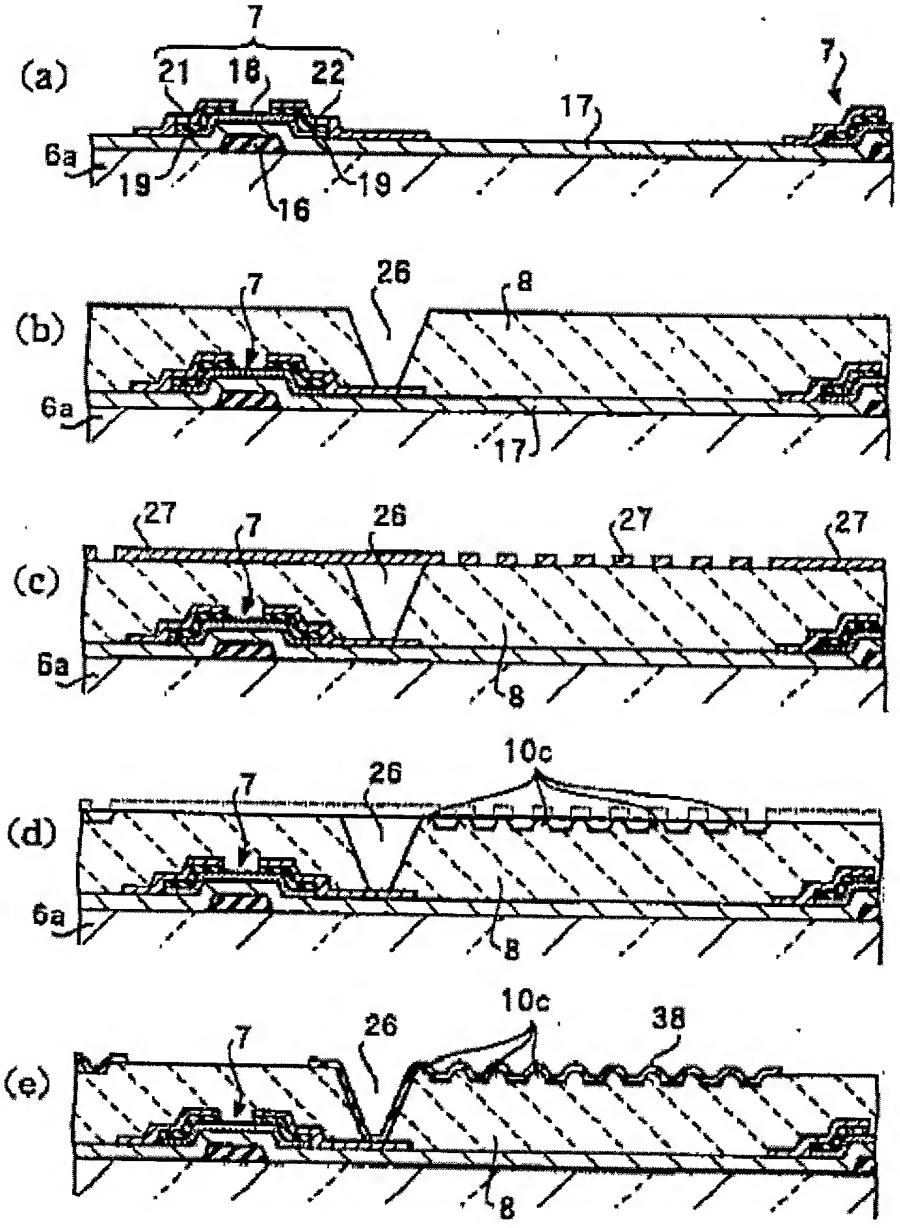

(a)
7
21
18
22
17
6a
19
16
19
(b)
7
26
8
6a
17
(c)
27
7
26
27
27
6a
8
(d)
10c
7
26
6a
8
(e)
10c
38
7
26
8

Fig. 7

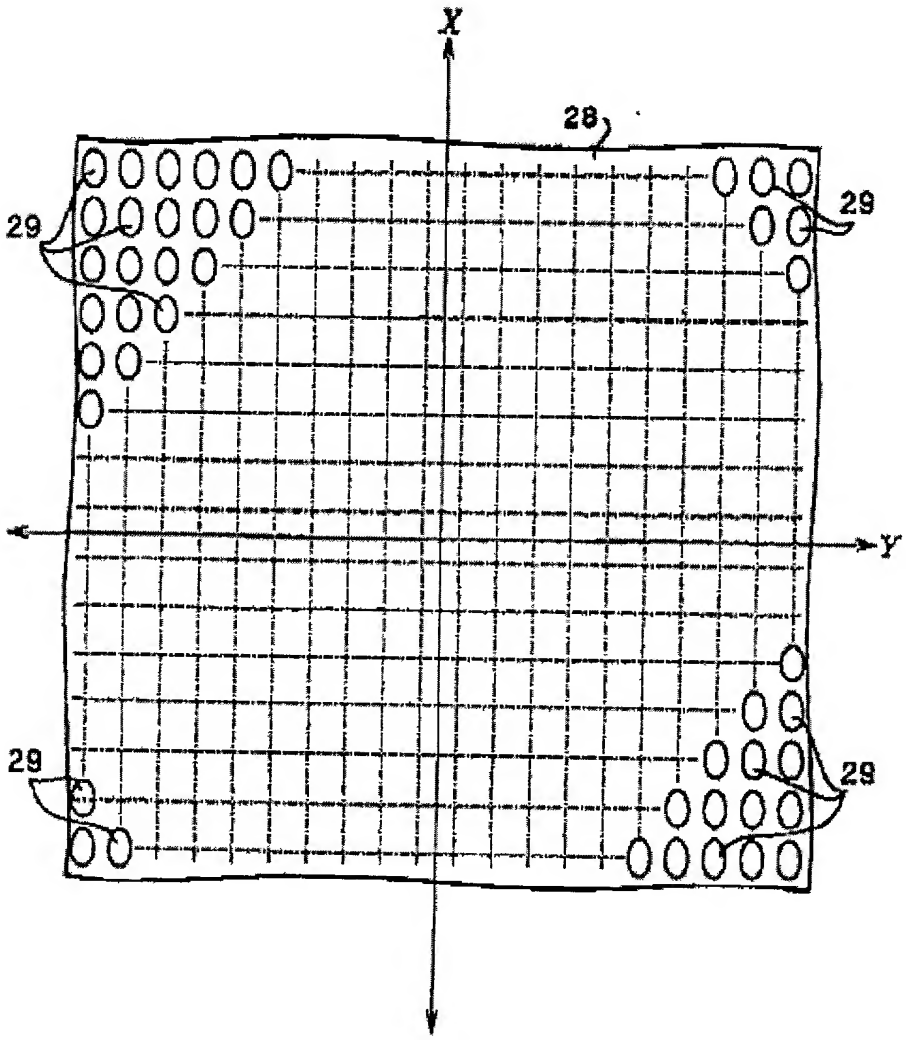


Fig. 8

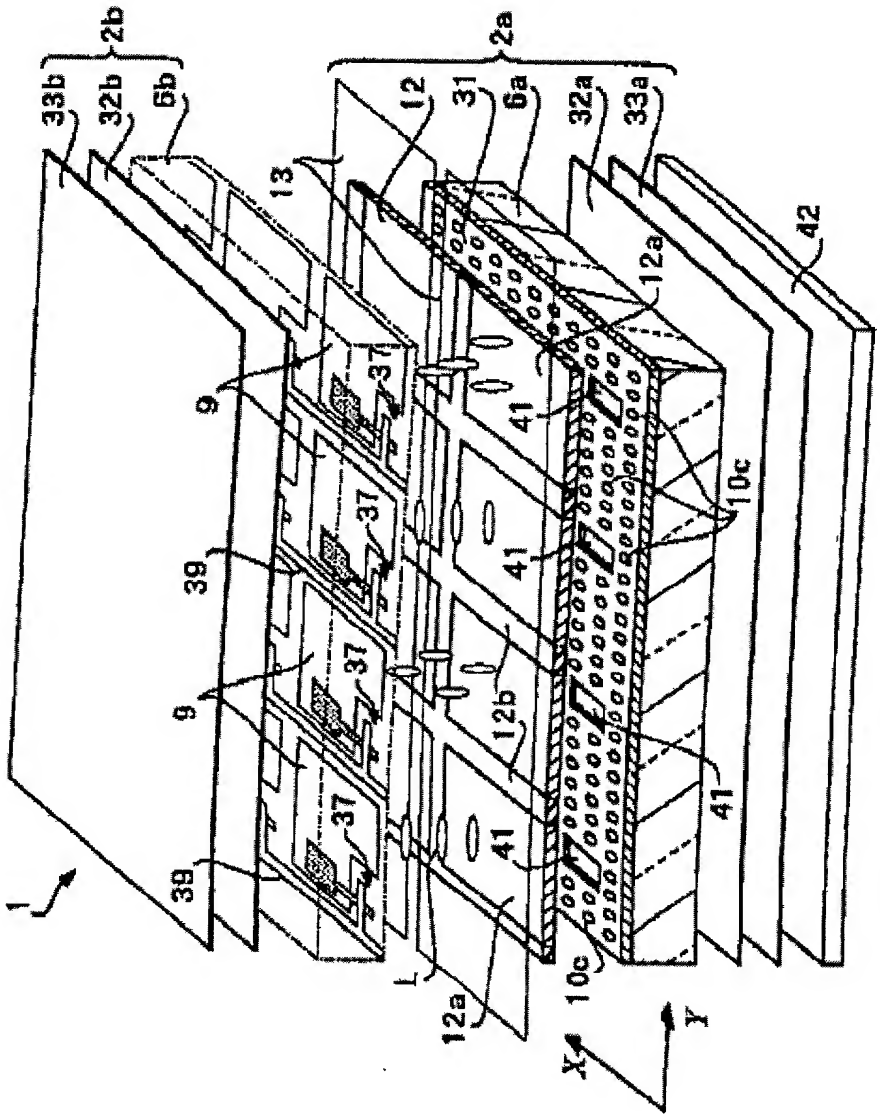


Fig. 9

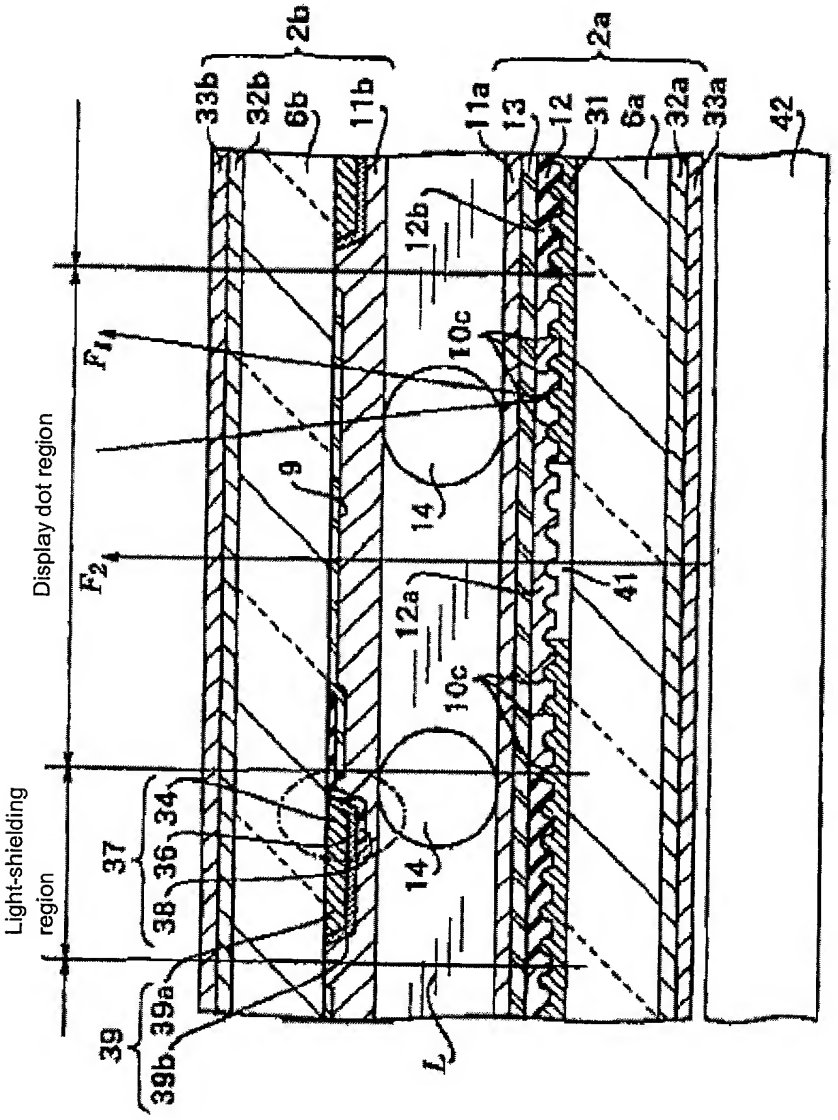

2b
2a
33b
32b
6b
11b
11a
13
12
31
6a
32a
33a
42
12b
10c
F_1
9
14
Display dot region
F_2
41
12a
10c
Light-shielding region
37
34
36
38
14
39
39a
39b
L

Fig. 10

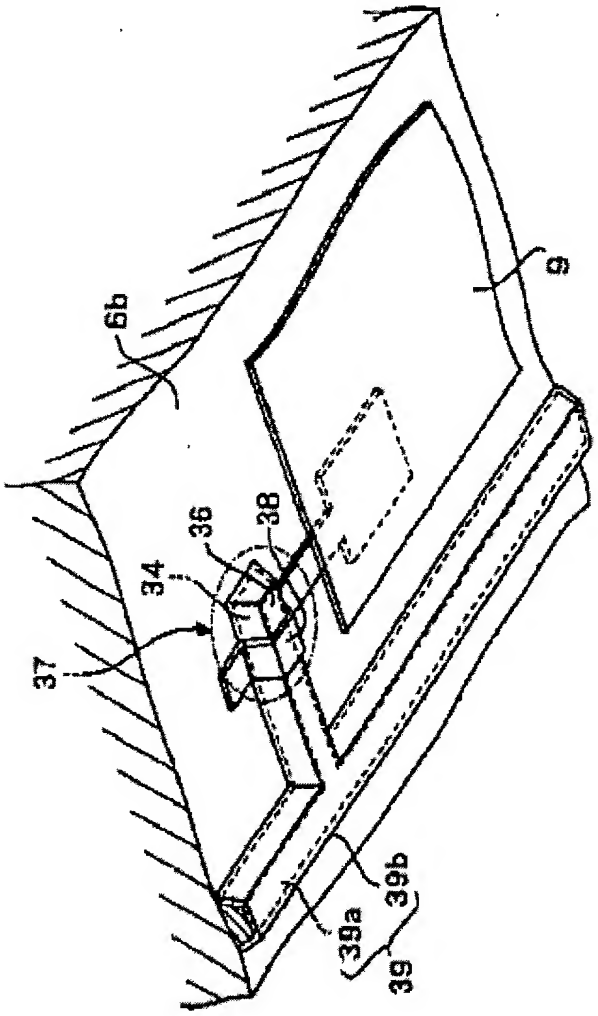


Fig. 11

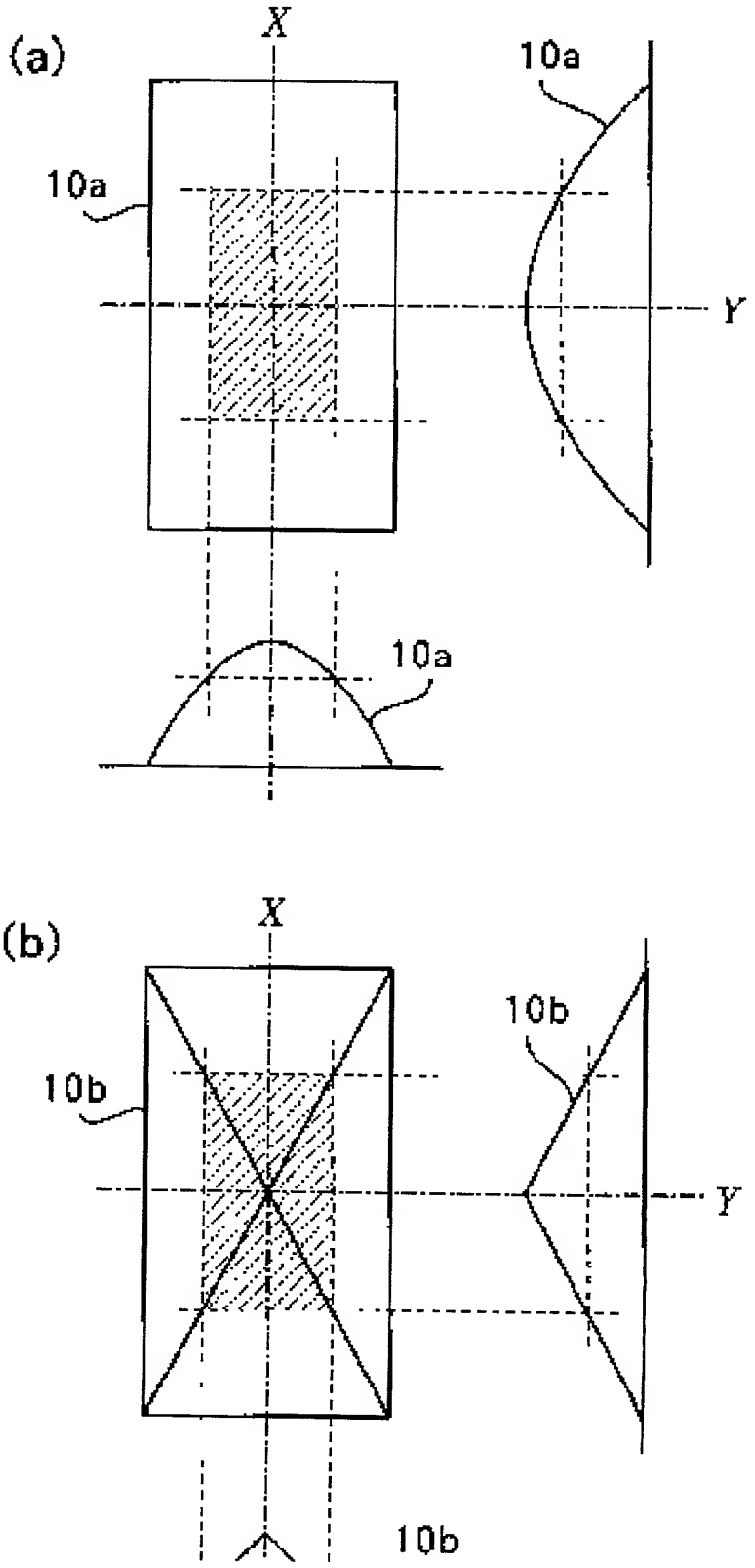
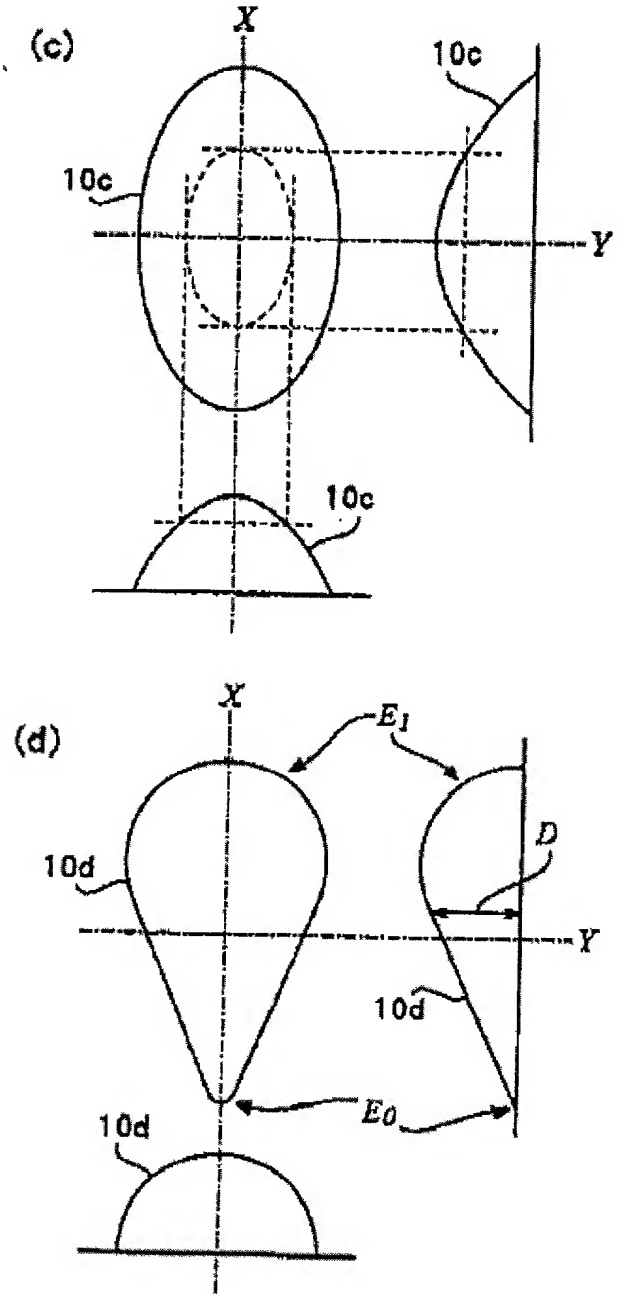


Fig. 12



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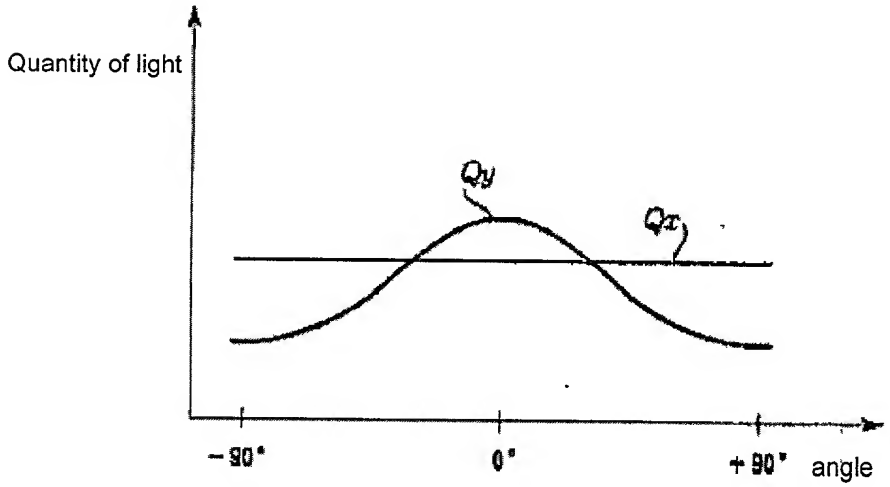


Fig. 14

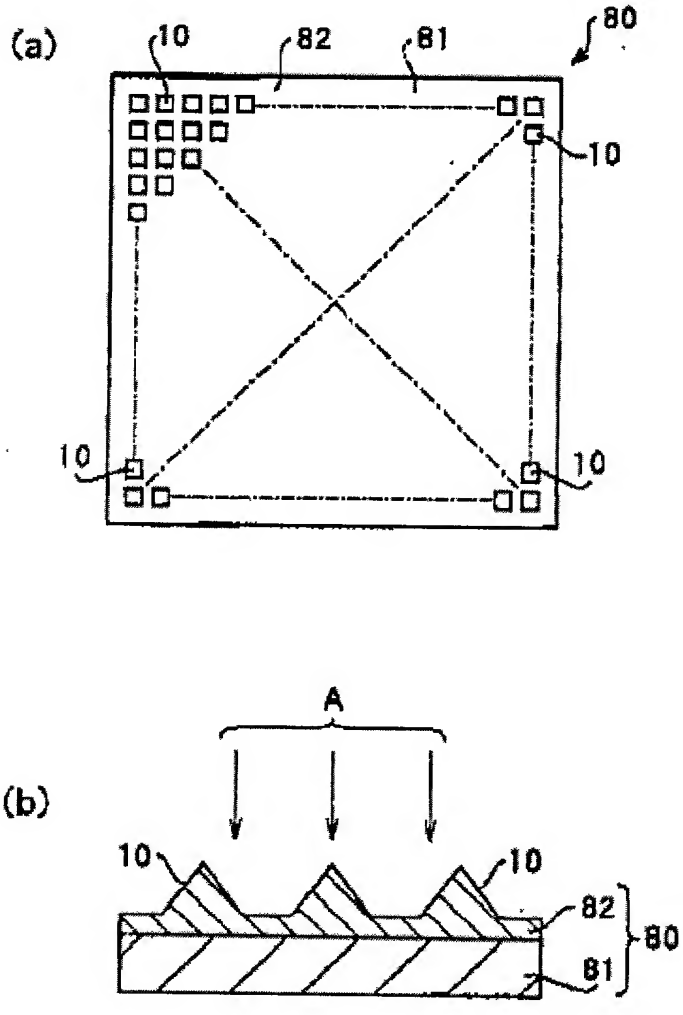


Fig. 15

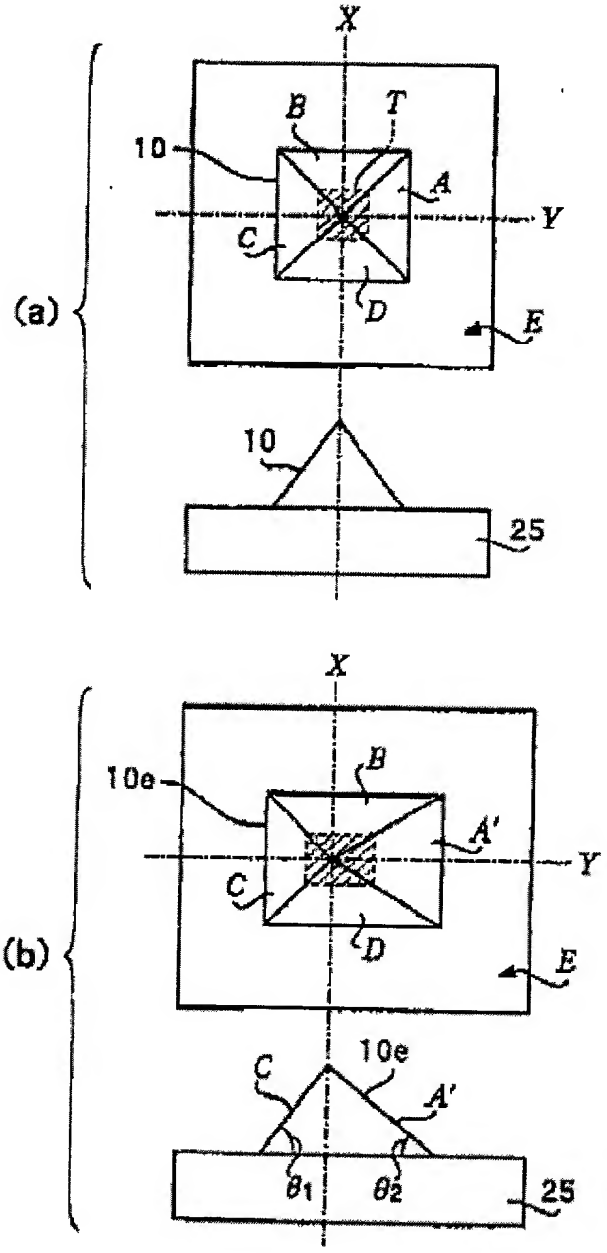


Fig. 16

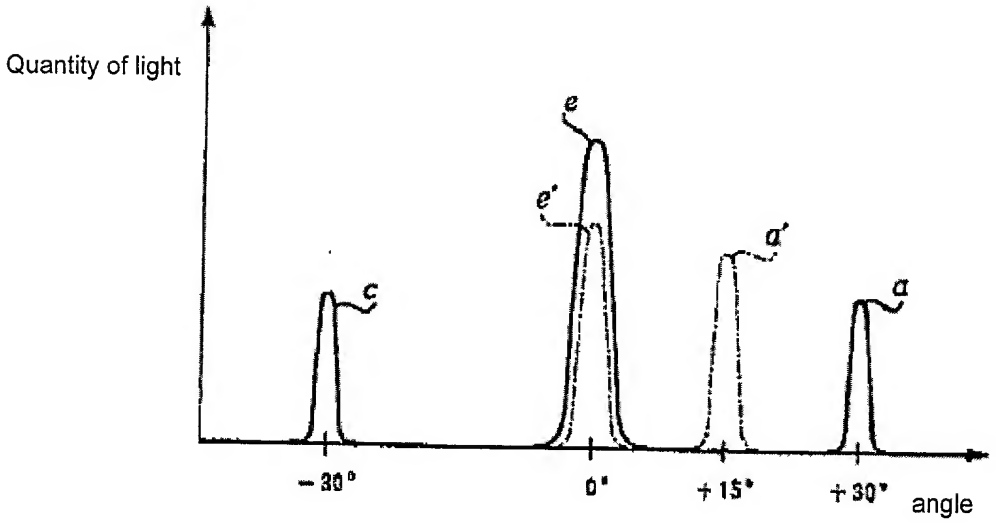


Fig. 17

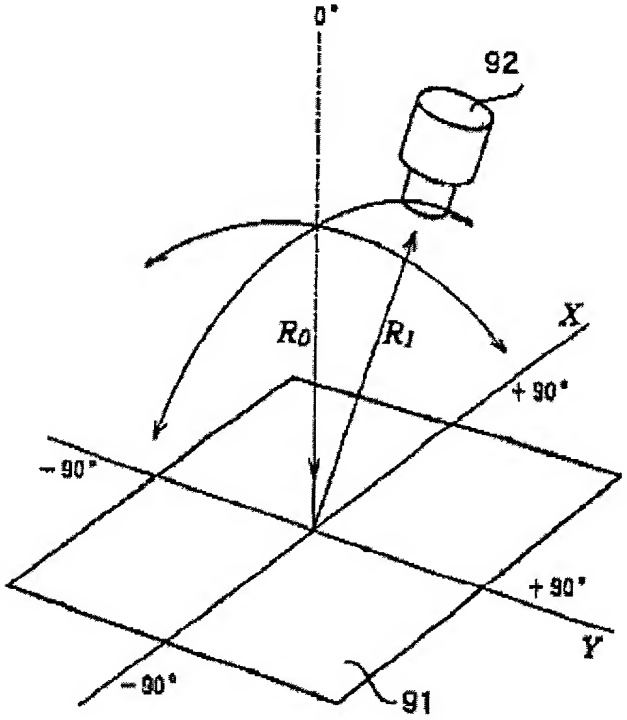


Fig. 18

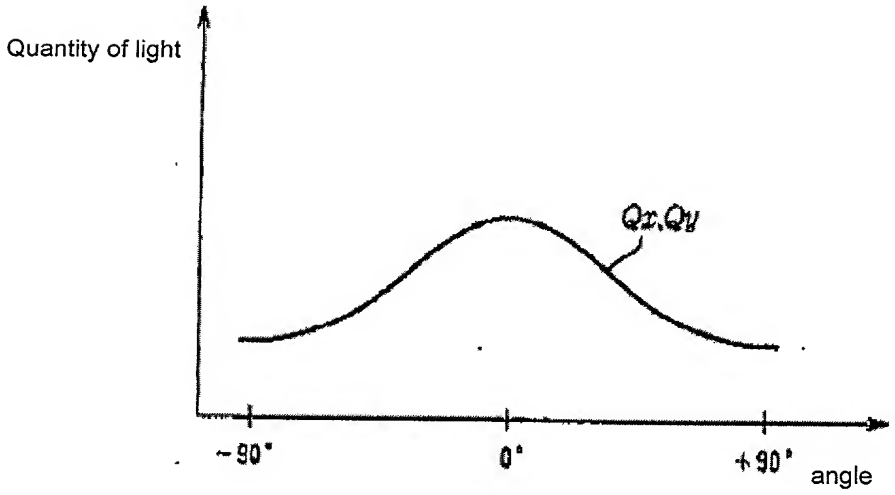


Fig. 19

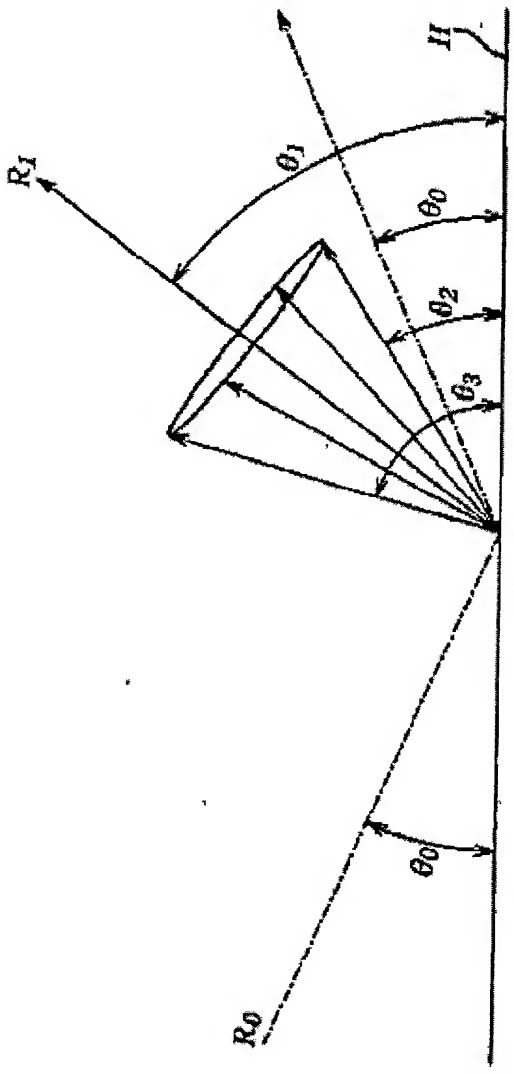


Fig. 20

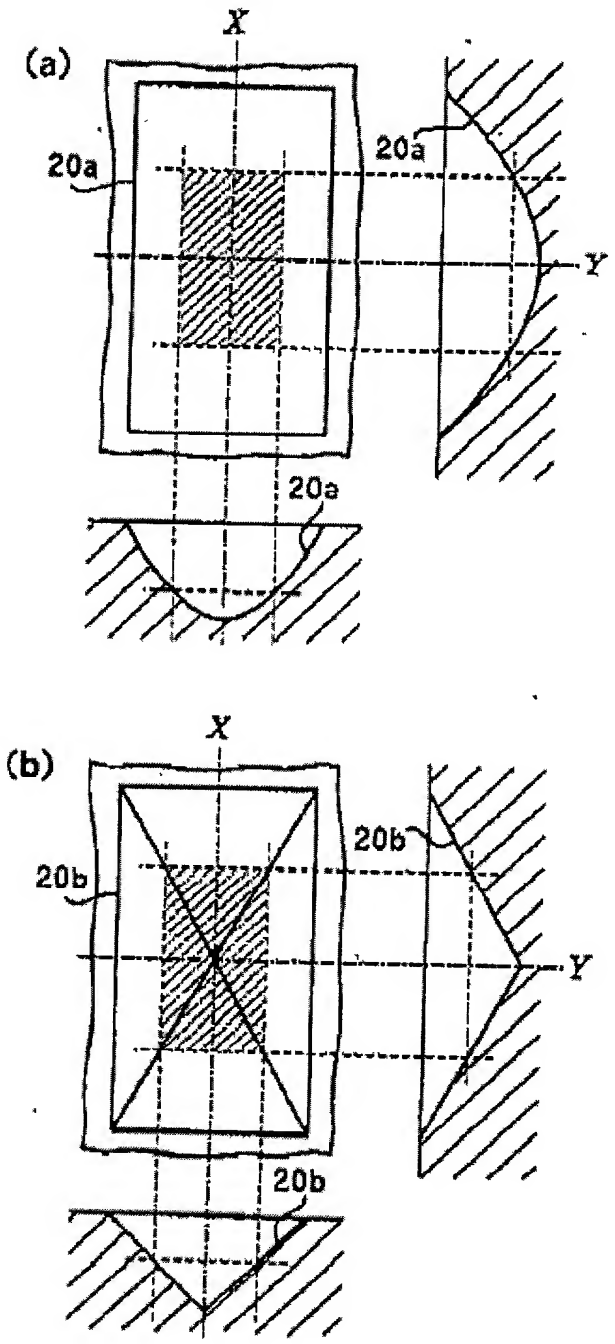


Fig. 21

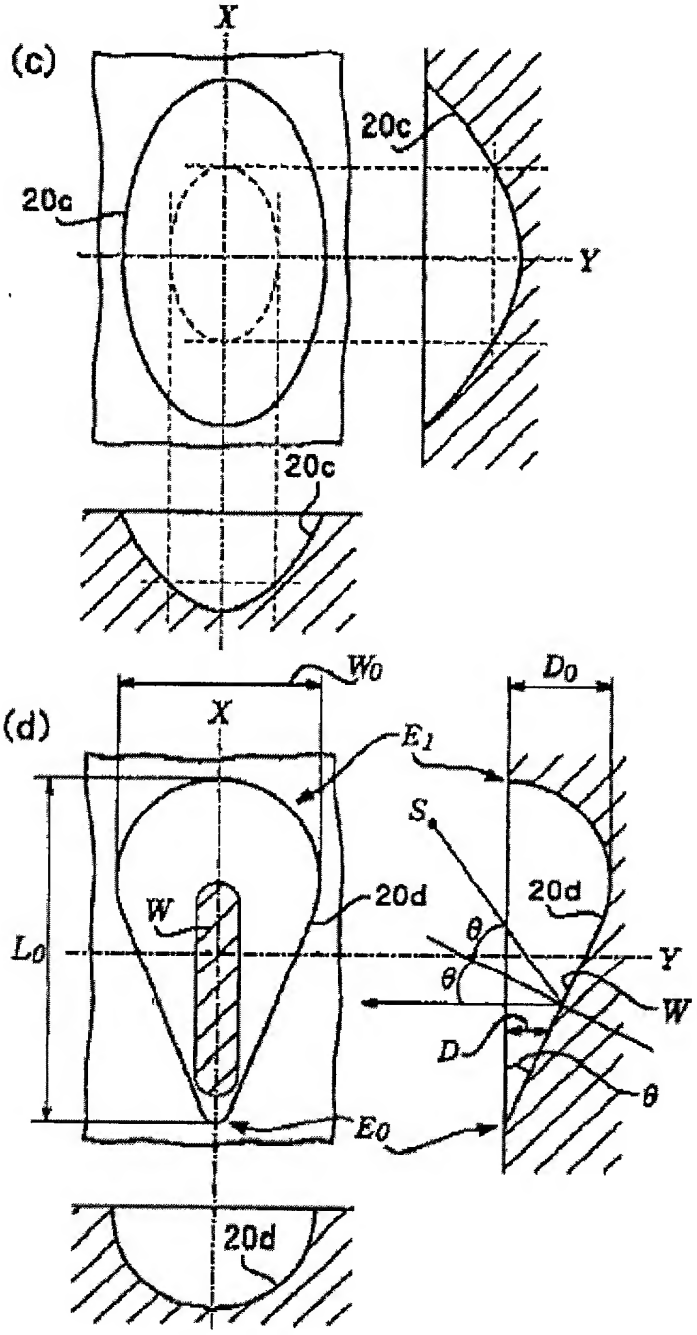


Fig. 22

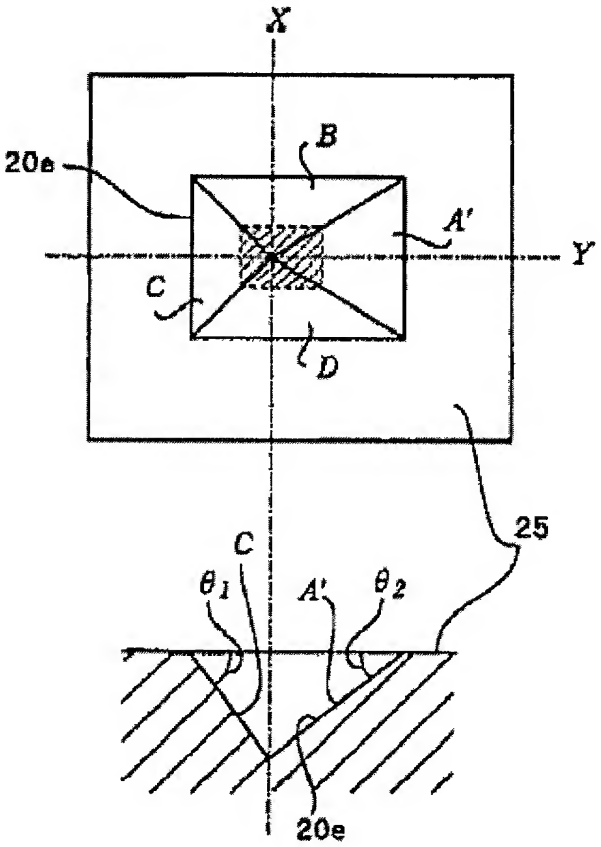


Fig. 23

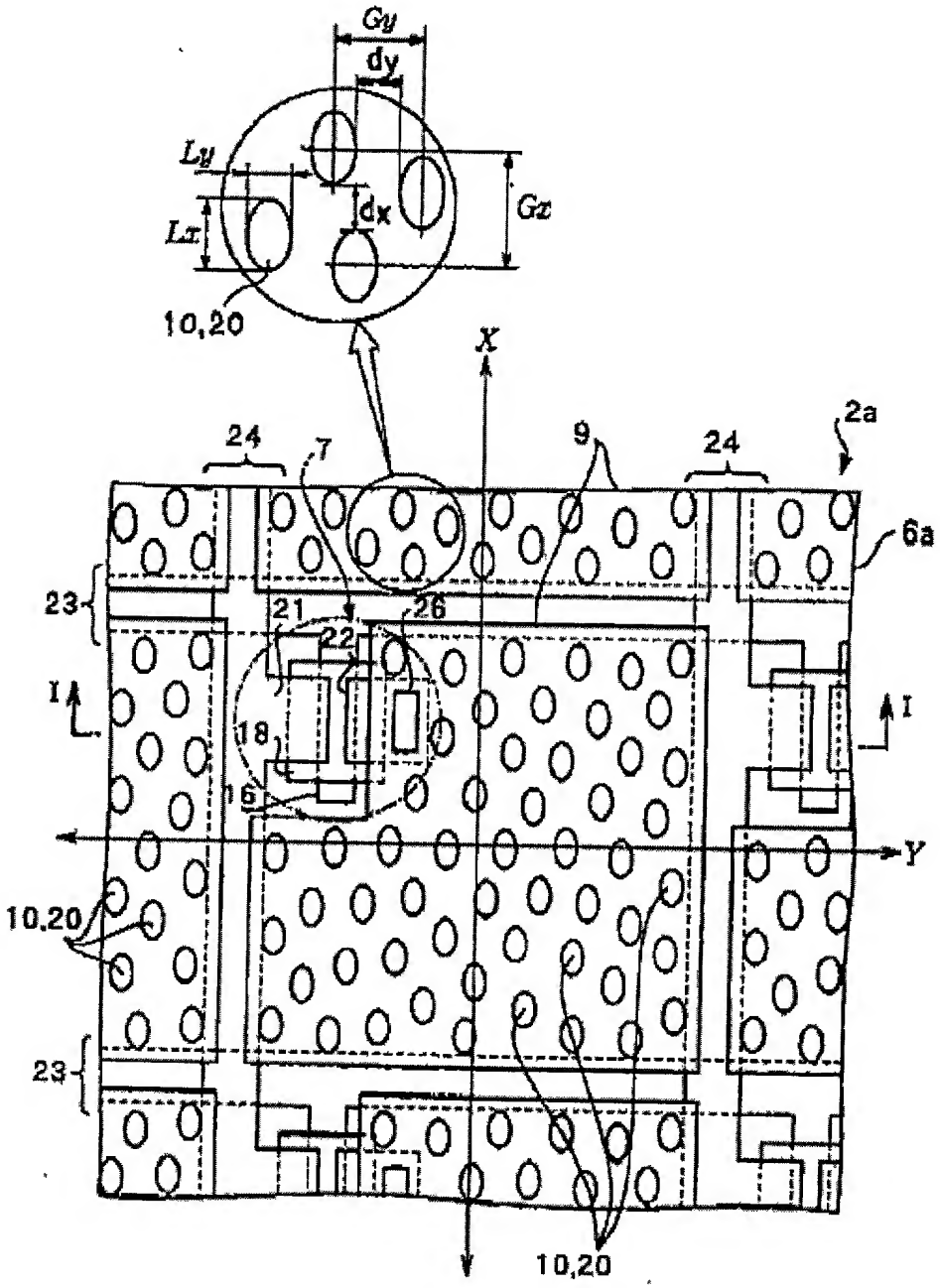

Gy
dy
Ly
dx
Gx
Lx
10,20
X
24
7
9
24
2a
6a
23
21
26
22
I
I
18
16
Y
10,20
23
10,20

Fig. 24

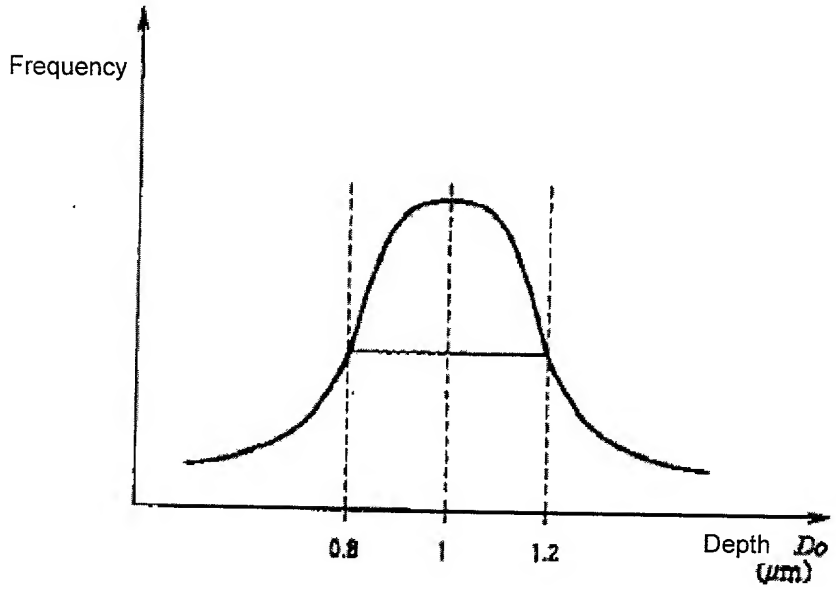


Fig. 25

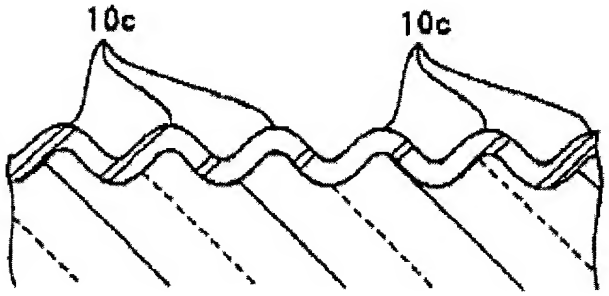


Fig. 26

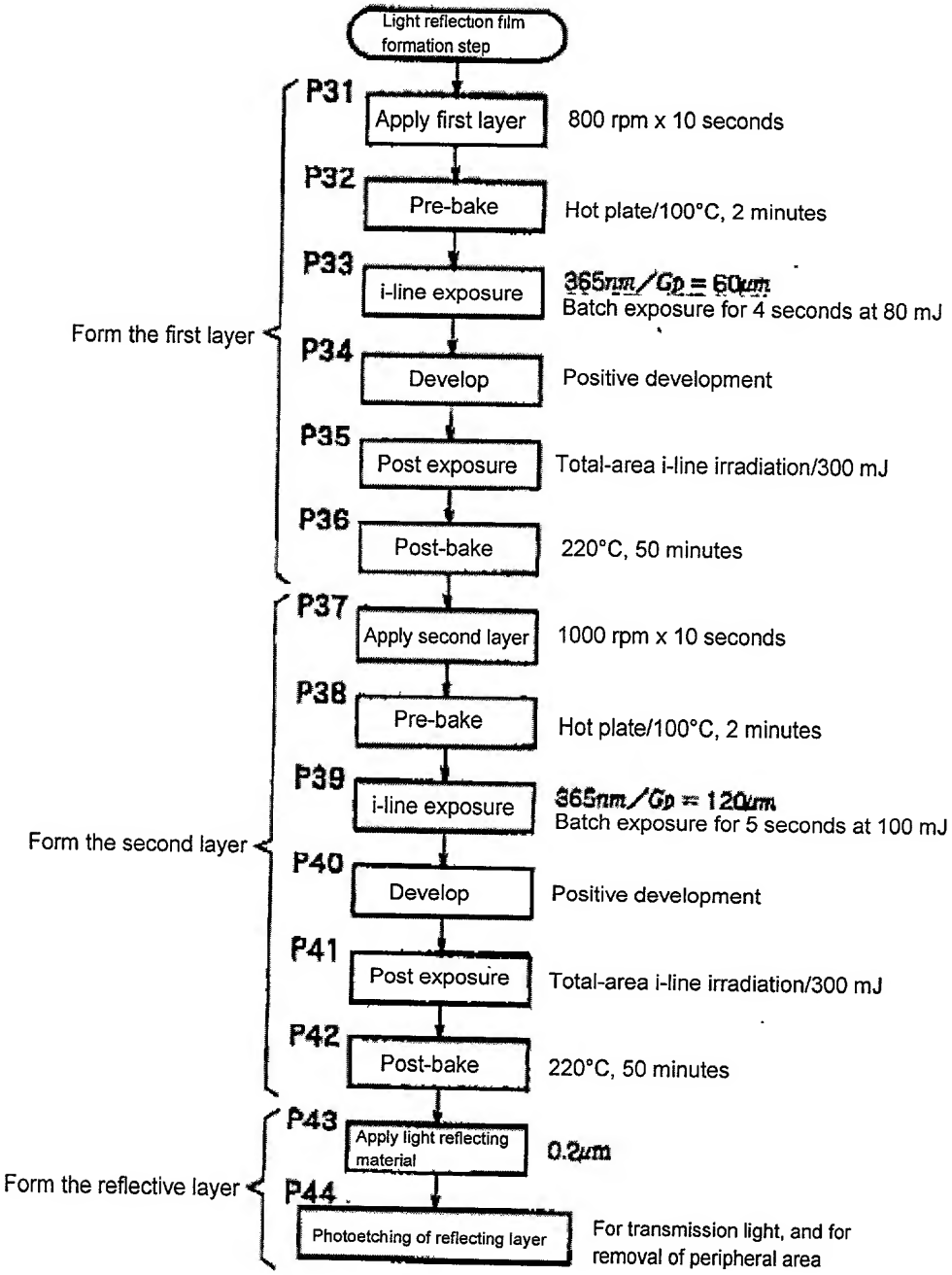

Light reflection film formation step
P31
Apply first layer
800 rpm x 10 seconds
P32
Pre-bake
Hot plate/100°C, 2 minutes
P33
i-line exposure
365nm/Gp = 60μm
Batch exposure for 4 seconds at 80 mJ
Form the first layer
P34
Develop
Positive development
P35
Post exposure
Total-area i-line irradiation/300 mJ
P36
Post-bake
220°C, 50 minutes
P37
Apply second layer
1000 rpm x 10 seconds
P38
Pre-bake
Hot plate/100°C, 2 minutes
P39
i-line exposure
365nm/Gp = 120μm
Batch exposure for 5 seconds at 100 mJ
Form the second layer
P40
Develop
Positive development
P41
Post exposure
Total-area i-line irradiation/300 mJ
P42
Post-bake
220°C, 50 minutes
P43
Apply light reflecting material
0.2μm
Form the reflective layer
P44
Photoetching of reflecting layer
For transmission light, and for removal of peripheral area

Fig. 27

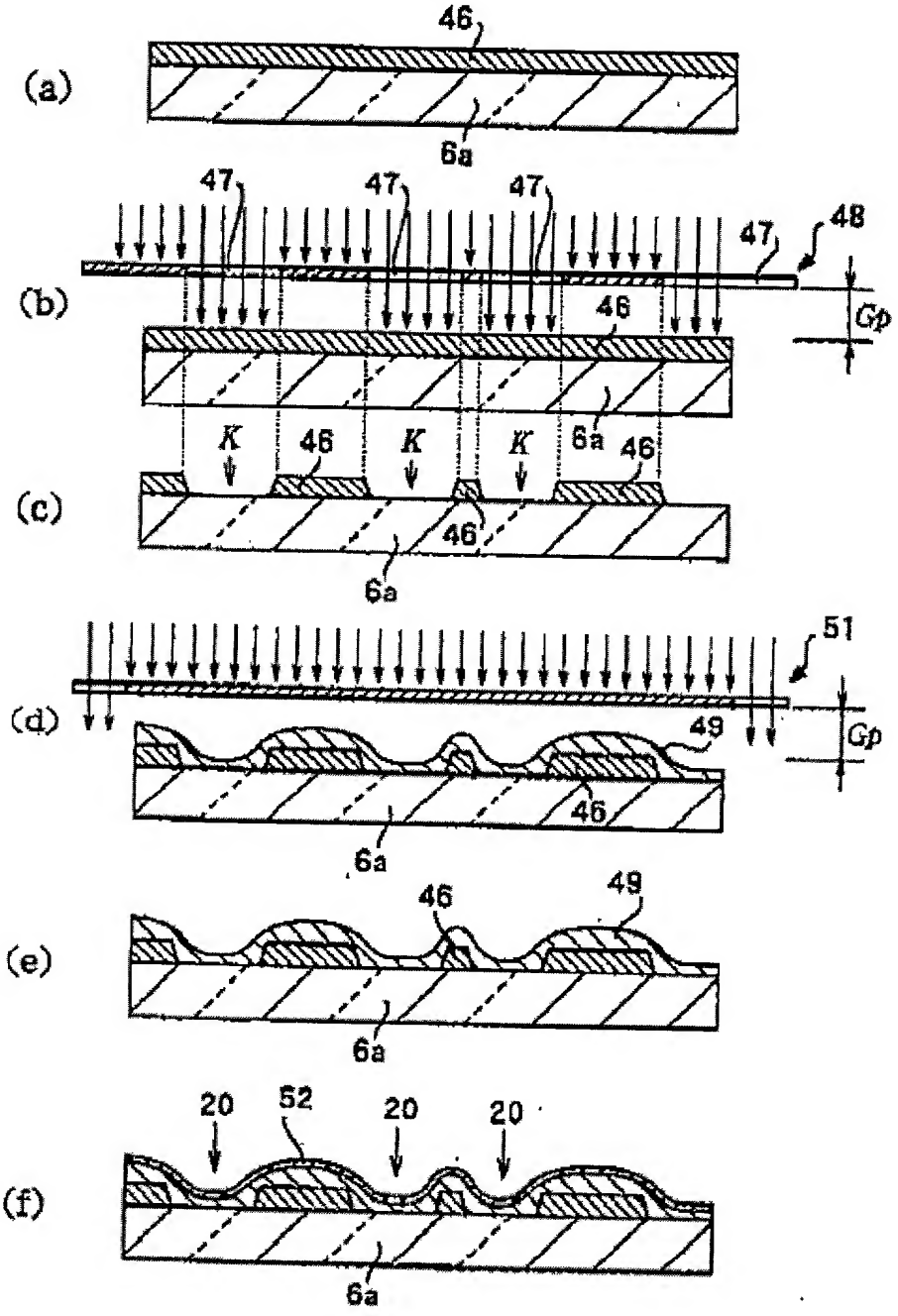

(a)
46
6a
(b)
47
47
47
47
48
Gp
46
6a
(c)
K
46
K
K
6a
46
46
6a
(d)
51
Gp
49
46
6a
(e)
46
49
6a
(f)
20
52
20
20
6a

Fig. 28

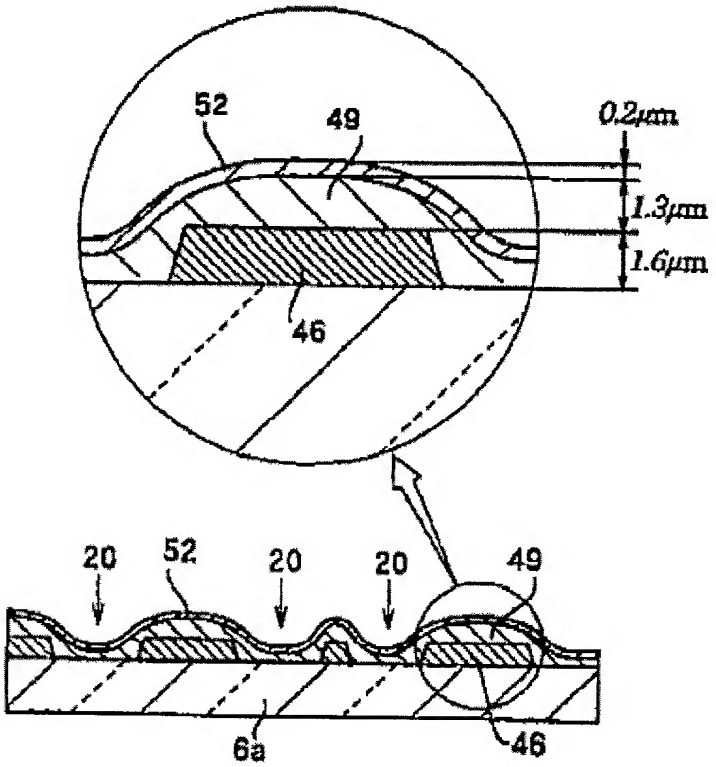


Fig. 29

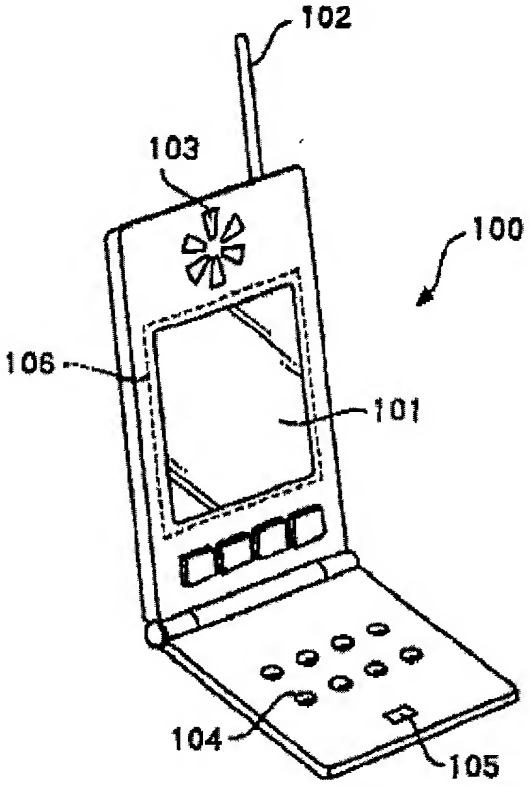


Fig. 30

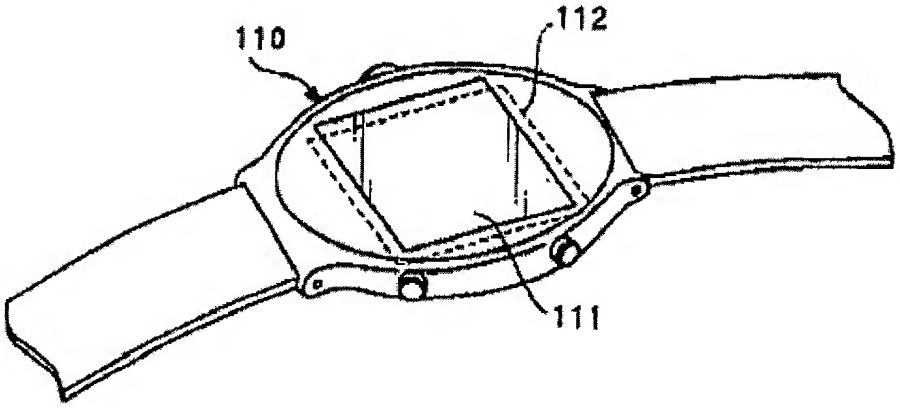


Fig. 31

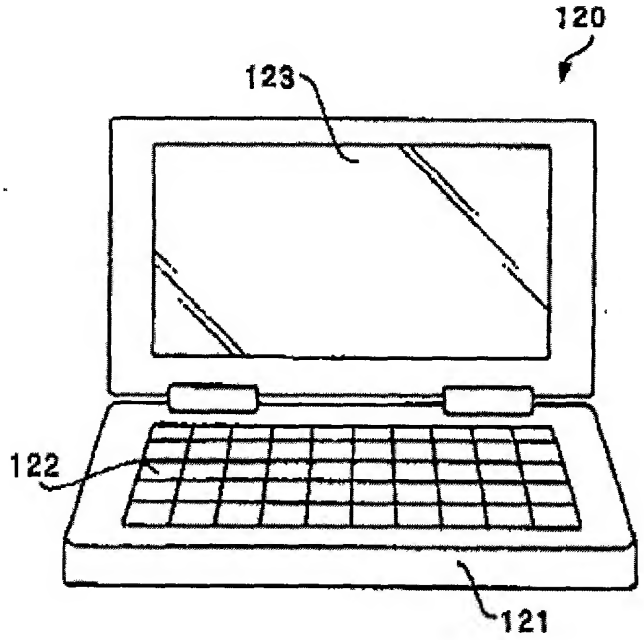
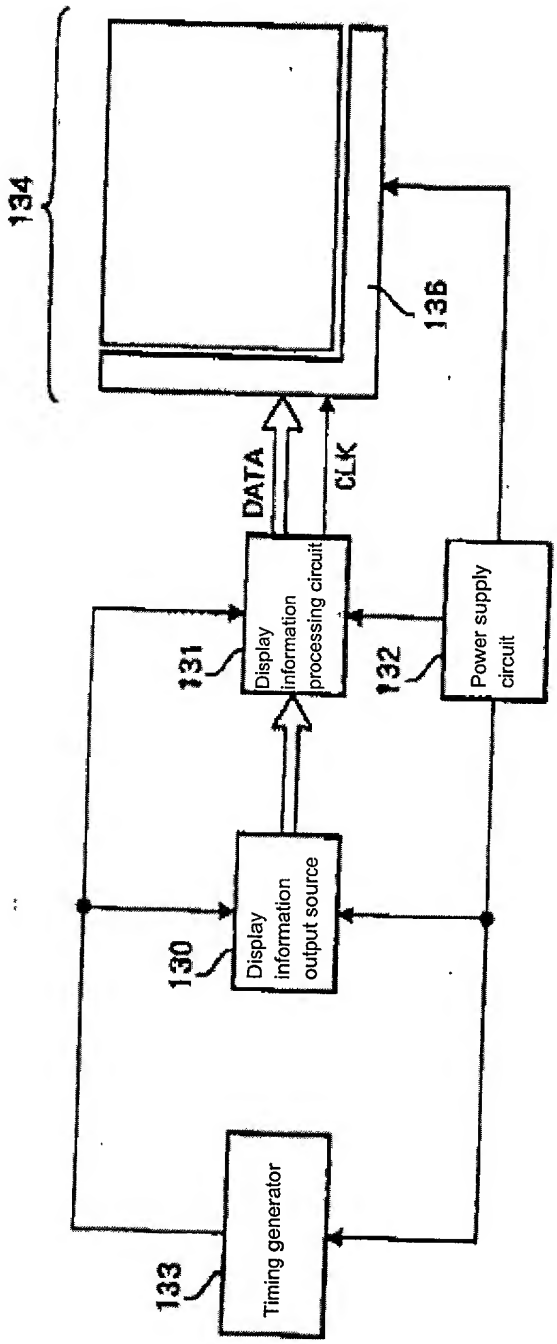


Fig. 32


134
136
DATA
CLK
131
Display information processing circuit
132
Power supply circuit
130
Display information output source
133
Timing generator